Ministry of Electronics and Information Technology (MeitY)
Govt. of India supports its
Electronics and ICT Academies to organize Faculty Development Programme on
VLSI Design Verification during 26th – 30th May, 2018 at
IIT Guwahati, IIT Roorkee, IIITDM Jabalpur, MNIT Jaipur, NIT Patna and NIT Warangal

About Summer Courses

Faculty Development Programmes in core areas of Electronics and Information & Communication Technology (ICT) streams have been planned by academies for delivery during Summer (i.e., May - June 2018). All these summer courses will be offered through National Knowledge Network (NKN) by inviting experts from IITs, NITs, IIITs and other premier institutes/industries. In addition, local course coordinators at respective academies /identified remote centers will take care of sessions on design oriented/activity linked problems/ assignments/ case studies and quiz test(s).

These courses will be delivered at E & ICT Academies/identified centers through NKN infrastructure. Candidates could apply for training at academy location or identified centers as per the convenience.

Course 2: VLSI Design Verification

Principal Coordinator Academy	Support Coordinator Academy	Participating Academies and Local Coordinator Details
Prof. Vineet Shaula vsahula@mnit.ac.in MNIT Jaipur	Dr. Gaurav Trivedi trivedi@iitg.ernet.in IIT Guwahati	MNIT Jaipur - *Prof. Vineet Sahula* vsahula@mnit.ac.in
		IIT Guwahati - *Dr. Gaurav Trivedi* trivedi@iitg.ernet.in
		IIITDM Jabalpur - *Prof. P.N. Kondekar* pnkondekar@iiitdmj.ac.in
		NIT, Warangal - *Dr. P Srihari Rao* patri@nitw.ac.in

Module details of VLSI Design Verification:

S.No.	Module Name	Topics
1.	Digital Design Flow	Introduction to VHDL/Verilog- Data types, Concurrent statements, sequential statements, behavioral modeling.
2.	Implementation	Introduction to programmable logic devices- PALs, PLDs, CPLDs and FPGAs.
3.	High Level Synthesis	Data path & Control Path, BDD, Scheduling, Resource Binding, Resource Allocation.
4.	Verification	Test benches, Formal Verification of digital hardware systems, FSM based Verification, CAD Tools for verification
5.	System Level Verification	System Verilog, Assertions & checkers, Coverage Driven Verification

Registration Fee: No Registration fee is charged for attending this programme planned at any designated academies/Remote centers. However, candidate should submit a refundable Demand Draft of Rs.1000/- along with application and the same will be handed over to participant on the last day of the training. Satisfactory Certificate will be given subject to fulfillment of attending all sessions, submission of assignments and clearing the test(s).

Last Date of Registration: 17th May'2018.

Lodging and Boarding will be provided free of cost at the Academy.

Participants can also attend the course at the following Remote Nodal Center

1.Maulana Azad National Institute of Technology (MANIT), Bhopal, Madhya Pradesh.

Remote Center Coordinator: Dr. Lalita Gupta

Email: gupta.lalita@gmail.com

2. DSPM- International Institute of Information Technology (DSPM-IIIT), Naya Raipur, Chhattisgarh

Remote Center Coordinator: Dr. Maoj Kumar Majumdar & Dr. Shrivishal Tripathi

Email: manojk@iiitnr.edu.in, shrivishal@iiitnr.edu.in.